## REMARKS

The specification has been amended to correct various self-evident errors in spelling, grammar, singular-versus-plural case, and reference-symbol usage. In addition, page 2 has been amended to refer to a pair of elements of the prior art voltage-controlled oscillator shown in application Fig. 2b but not mentioned in the specification. On page 8, the doping types and level have been corrected for certain of the doped regions in the description of Wong's prior art varactor of application Fig. 7.

In the paragraph bridging pages 9 and 10, "maximum-to-minimum varactor ratio" has been changed to "maximum-to-minimum capacitance ratio" to be consistent with the earlier usage of "maximum-to-minimum capacitance ratio" in that paragraph. On page 28, "p-n junction 152" has been corrected to "plate region 152". On page 47, "plate electrode 162" has been corrected to "gate electrode 162".

On page 57, reference symbols "260", "262", "264", "266", and "268" for the curves shown in application Figs. 20a and 20b have been respectively changed to "266", "268A", "268B", "268C", and "268D" since each of reference symbols "260" and "262" is employed earlier in the specification to identify an item other than a curve. On pages 59 and 60, the expressions "plate voltage $v_G$", "plate voltage $V_G$", and "plate voltage $v_g$" have been respectively changed to "gate voltage $v_G$", "gate voltage $V_G$", and "gate voltage $v_g$" since the subscript "G" or "g" is used to identify a gate parameter.

On page 61, the expression "Fig. 7" has been changed to "varactor of Fig. 8" because the varactor operation described earlier in the sentence referring to "Fig. 7" clearly means the operation of the varactor of application Fig. 8. On page 70, "14" has been changed to "fourteen" to avoid having "14" being misconstrued as a reference symbol.

Turning to the claims, Claims 1 - 16 have been cancelled. Claims 17, 23, 32, 36, and 38 have been amended. Claims 47 - 66, including independent Claim 63, have been added. Accordingly, Claims 17 - 66 are now pending.

LAW OFFICES OF
SKJERVEN MORRILL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Insofar as the revisions to Claims 17 and 23 are concerned, these two claims have been amended to provide that the recited elements are elements of a varactor so as to facilitate the addition of respective new dependent Claims 47 and 55 which refer to the varactor. The

revisions to Claims 17 and 23 do not change their scope. The revision to Claim 38 deletes an element, the plate electrode, which was recited in the definite sense in the deleted material but was not earlier defined in the claim.

Claims 22, 31 - 34, 36, 37, and 42 have been rejected under 35 USC 102(b) as anticipated by Ikeda et al ("Ikeda"), U.S. Patent 5,497,028. Claims 17 - 21, 23 - 30, 38 - 41, and 43 - 46 have been rejected under 35 USC 103(a) as obvious based on Ikeda as applied to Claim 1 and further in view of Sedra et al ("Sedra"), Microelectronic Circuits, 1998, page 382. Claim 35 has been rejected under 35 USC 103(a) as obvious based on Ikeda as applied to Claim 32 and further in view of Imoto et al. ("Imoto"), U.S. Patent 6,166,404. These rejections are respectfully traversed.

As a preliminary matter, Claims 22, 31, and 42 rejected on the basis of Ikeda respectively depend (directly or indirectly) from independent Claims 17, 23, and 38 rejected on the basis of Ikeda and Sedra. Inasmuch as dependent Claims 22, 31, and 42 thus respectively include all the limitations of Claims 17, 23, and 38, Applicants' attorney does not understand how Claims 22, 31, and 42 can be rejected solely on the basis of Ikeda. Accordingly, Applicants' attorney assumes that the Examiner intended to reject Claims 22, 31, and 42 as obvious under 35 USC 103(a) based on Ikeda in view of Sedra.

Independent Claim 17 is directed to a structure containing a gate-enhanced junction varactor whose gate-to-body voltage is maintained approximately constant as the varactor's plate-to-body voltage is varied. Independent Claim 23 is directed to a structure containing a gate-enhanced junction varactor whose gate-to-body voltage differs from the varactor's plate-to-body voltage and whose gate-to-body voltage is varied as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

Referring to Claims 17, 23, and certain other claims, the Examiner alleges in the paragraph bridging pages 2 and 3 of the Office Action that "Ikeda discloses the claimed invention except the plate to body bias voltage and the gate to body voltage is varied as a function of the plate to body voltage". In making this allegation, the Examiner is presumably referring to page 1 of the Office Action where the Examiner analogizes elements of a varactor to the elements of field-effect transistor ("FET") 53 in Fig. 50C of Ikeda. The Examiner continues in the paragraph bridging pages 2 and 3 of the Office Action to allege that "Sedra

LAW OFFICES OF
SKJERVEN MORRILL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

discloses on page 382, figure 5.25, a FET transistor in which the drain plate and the gate are biased by a voltage VD, hence gate to body voltage is varied linearly, by a constant multiplier of 1, as a function of the plate to body voltage as the plate to body voltage is varied". Finally, the Examiner alleges that "Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to connect the plate region in Ikeda's invention to the gate region, thus make a signal path, and further bias them together with a voltage, or separately bias the plate and the gate relative to the body in order to control the operation of the transistor".

FET 53 in the circuitry of Fig. 50C of Ikeda is a p-channel FET as indicated at col. 27. The source and body region of FET 53 are connected together to a high voltage supply. The drain of FET provides the output signal of the circuitry and is coupled through a resistor to ground.

In Fig. 50C of Ikeda, the gate electrode of FET 53 is connected to inductance-capacitance (LC) element 106. FETs can be controlled in many ways. The way in which FET 53 is controlled in the circuitry of Fig. 56C of Ikeda depends on the function to be performed by inductance-capacitance element 100. At col. 27, Ikeda specifies that the illustrated FET, i.e., FET 53, is provided with reveres bias so that the FET functions as a buffer.

Claim 17 requires that the gate-to-body voltage be maintained approximately constant as the plate-to-body voltage is varied. Since the body region of FET 53 in Fig. 50C of Ikeda is connected to the high voltage supply, attempting to maintain the gate-to-body voltage approximately constant for FET 53 would mean that the voltage applied from inductance-capacitance element 100 to the gate electrode of FET 53 would be approximately constant. The output signal from the drain of FET 53 would then similarly be at an approximately constant value. As a result, the circuitry in Fig. 50C would perform no function.

In other words, controlling FET 53 in Fig. 50C so that the gate-to-body voltage of FET 53 is approximately constant would be a useless way of controlling FET 53. No person skilled in the art would attempt to control FET 53 in that way. Regardless of what Sedra says about controlling FETs, nothing in Ikeda and Sedra would provide a person skilled in the art

LAW OFFICES OF
SKJERVEN MORRILL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

with any incentive for applying Sedra to Ikeda so as to achieve the subject matter of Claim 17. Accordingly, Claim 17 is patentable over Ikeda and Sedra.

Claims 18 - 22 depend (directly or indirectly) from Claim 17. The same applies to new Claims 47 - 54. Dependent Claims 18 - 22 and 47 - 54 are thus patentable over Ikeda and Sedra for the same reasons as Claim 17.

Claim 23 requires that the gate-to-body voltage differ from the plate-to-body voltage and that the gate-to-body voltage be varied as a function of the plate-to-body voltage as the plate-to-body voltage is varied. The voltage supplied from inductance-capacitance element 100 to the gate electrode of FET 53 in Fig. 50C of Ikeda is the input voltage to FET 53. Irrespective of whether the Examiner is analogizing (a) the drain-to-body voltage of FET 53 to the plate-to-body voltage of Claim 23 or the (b) source-to-body voltage of FET 53 to the plate-to-body voltage of Claim 23, the so-analogized plate-to-body voltage of FET 53 clearly varies as a function of the gate-to-body voltage rather than, as required in Claim 23, having the gate-to-body voltage vary as a function of the plate-to-body voltage.

Stated differently, inductance-capacitance element 100 and FET 53 in Fig. 50C of Ikeda are not configured to enable the gate-to-body voltage to vary as a function of the plate-to-body voltage regardless of whether the Examiner is analogizing the plate-to-body voltage of Claim 23 to the drain-to-body or source-to-body voltage of FET 53. As with Claim 17 and thus regardless of what Sedra discloses about controlling FETs, nothing in Ikeda and Sedra would provide a person skilled in the art with any motivation for applying Sedra to Ikeda in such a way as to attain the subject matter of Claim 23. Consequently, Claim 23 is patentable over Ikeda and Sedra.

Claims 24 - 31 depend (directly or indirectly) from Claim 23. New Claims 55 - 62 likewise depend (directly or indirectly) from Claim 23. Hence, dependent Claims 24 - 31 and 55 - 62 are patentable over Ikeda and Sedra on the same basis as Claim 23.

Turning to independent Claim 32, it has been amended to provide that the plate region comprises a main plate portion and a plurality of finger portions. Claim 32 thus essentially constitutes the original version of Claim 36 rewritten in independent form.

LAW OFFICES OF
SKJERVEN MORRILL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

In rejecting Claims 32 and 36 as anticipated by Ikeda, the Examiner says on page 2 of the Office Action that "Ikeda discloses in figure 46 electrode 26 and source 12 corresponding to the plate region are finger shaped".

Source 12 in Fig. 46 of Ikeda is illustrated as having a main portion and a narrower portion continuous with the main portion. The same applies to drain 14 in Fig. 46. However, neither source 12 nor drain 14 in Fig. 46 consists of a main portion and plurality of, i.e., two or more, narrower portions continuous with the main portion. Nor is source 12 or drain 14 disclosed anywhere else in Ikeda as consisting of a main portion and a plurality of narrower portions continuous with the main portion. Hence, Ikeda did not anticipate the original version of Claim 36 and does not anticipate amended Claim 32.

Furthermore, nothing in Ikeda would provide a person skilled in the art with any reason for configuring source 12 or drain 14 in any of Ikeda's implementations to consist of a main portion and a plurality of narrower portions continuous with the main portion. Accordingly, Claim 32 is patentable over Ikeda.

Claims 33, 34, 36, and 37 all depend from Claim 32. Hence, Claims 33, 34, 36, and 37 are patentable over Ikeda on the same basis as Claim 32.

Claim 35, which has been rejected as obvious based on Ikeda and Imoto, likewise depends from Claim 32. While Imoto does disclose recessed isolation region 81, Imoto does not disclose that the source or drain of an FET is laterally configured to consist of a main portion and a plurality of narrower portions continuous with the main portion. Even it were reasonable to combine Ikeda and Imoto in the manner proposed by the Examiner, the combination of the two references would not teach the full subject matter of Claim 35. Consequently, Claim 35 is patentable over Ikeda and Imoto.

Independent Claim 38, which has been rejected as obvious based on Ikeda and Sedra, is directed toward designing a gate-enhanced junction varactor. Claim 38 specifies that the plate and inversion areas are controlled to control the minimum and maximum capacitances of the varactor.

LAW OFFICES OF
SKJERVEN MORRILL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Nowhere does Ikeda mention anything about controlling any areas so as to control the minimum and maximum values of any of the capacitors employed in Ikeda's circuitry. Nor

does Sedra mention anything about controlling any areas to control minimum and maximum capacitance values. Even if it were reasonable to combine Ikeda and Sedra in the proposed manner, the combination would not teach the full subject matter of Claim 38. For this reason, Claim 38 is patentable over Ikeda and Sedra.

Claims 39 - 46 depend (directly or indirectly) from Claim 38. Hence, dependent Claims 39 - 46 are patentable over Ikeda and Sedra for the same reasons as Claim 38.

New independent Claim 63 is directed to a structure containing a gate-enhanced junction varactor in which (a) the body contact portion of the body region is more heavily doped than the surface depletion region and (b) the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion. As far as Applicants' attorney can determine, Ikeda does not disclose any structure having these two features along with the other features of Claim 63. Even if it were reasonable to combine Ikeda with Sedra or/and Imoto, the combination would not teach a structure having the full subject matter of Claim 63. As a result, Claim 63 is patentable over Ikeda, separately or in combination Sedra or/and Imoto. The same applies to new Claims 64 - 66 since they depend from Claim 63.

In short, Claims 17 - 66 are patentable over the applied art. Accordingly, Claims 17 - 66 should be allowed so that the application may proceed to issue.

Please telephone applicant's attorney at 408-453-9200, ext. 1371, if there are any questions.

EXPRESS MAIL LABEL NO.:

EL 901 565 502 US

Respectfully submitted,

Ronald J. Meetin

Ronald J. Meetin
Attorney for Applicant
Reg. No. 29,089

LAW OFFICES OF
SKJERVEN MORRILL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

APPENDIX

CLAIMS 17, 23, 32, 36, AND 38,
WITH ANNOTATIONS TO INDICATE REVISIONS,
OF U.S. PATENT APPLICATION 09/903,059
ATTY DOCKET NO. NS-4971 US

17. (Amended) A structure comprising a varactor which comprises:

a plate region and body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

a plate electrode and a body electrode respectively connected to the plate and body regions, the plate electrode being at a plate-to-body bias voltage relative to the body electrode;

a dielectric layer situated over the semiconductor body and contacting the body region; and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the gate electrode being at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage being maintained approximately constant as the plate-to-body voltage is varied.

23. (Amended) A structure comprising a varactor which comprises:

a plate region and body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

a plate electrode and a body electrode respectively connected to the plate and body regions, the plate electrode being at a plate-to-body bias voltage relative to the body electrode;

a dielectric layer situated over the semiconductor body and contacting the body region; and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the gate electrode being at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage differing from the plate-to-body voltage,

the gate-to-body voltage varying as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

32. (Amended) A structure comprising:

a plate region and a body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions extending to a primary surface of the semiconductor body and meeting each other to form a p-n junction, the plate region comprising a main plate portion and a plurality of finger portions [at least one finger portion] continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong;

a dielectric layer situated over the semiconductor body and contacting the plate region; and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region.

36. (Amended) A structure as in Claim 32 wherein two of the finger portions extend longitudinally largely perpendicular to each other [there are at least two finger portions].

38. (Amended) A method comprising:

selecting a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a dielectric layer situated over the semiconductor body and contacting the body region, and (c) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region occurring in the body region [under control of the plate and gate electrodes], the inversion layer occupying a lateral inversion area along the

primary surface, the varactor having a maximum capacitance dependent on the inversion area in combination with the plate area; and

adjusting the plate and inversion areas to control the minimum and maximum capacitances of the varactor.